IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Shinji Ohuchi et al. Group Art Unit: 2814

Serial No.: 10/657,139 Examiner: D. Nguyen

Filed: September 9, 2003 Confirm. No.: 1910

For: SEMICONDUCTOR DEVICE INCLUDING SEMICONDUCTOR ELEMENTS MOUNTED ON BASE PLATE

AMENDMENT

U.S. Patent and Trademark Office
****Via efiling****
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Date: February 20, 2008

Sir:

In response to the Final Office Action dated August 21, 2007, the period for response having been extended an additional two (2) months to February 21, 2008, the following amendments and remarks are respectfully submitted, concurrently along with a Request for Continued Examination (RCE), in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-33 (Canceled)

Claim 34 (Previously Presented): A semiconductor device comprising:

a BGA (ball grid array) type semiconductor device including a base plate and a plurality of bumps formed on a backside surface of the base plate; and

a CSP (chip size packaged) type semiconductor device mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have the plurality of bumps formed thereon,

said CSP type semiconductor device having a semiconductor element which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals which are formed on the main surface,

wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed,

wherein the backside surface of the base plate is mounted to a printed circuit board via the plurality of bumps, and said CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of the

plurality of bumps, and

wherein said CSP type semiconductor device has a resin that covers the main surface of the semiconductor element and side surfaces of the terminals.

Claim 35 (Previously Presented): The semiconductor device of claim 34, wherein the plurality of terminals of said CSP type semiconductor device are electrically connected to the plurality of bumps via wiring patterns formed on the backside surface of the base plate.

Claim 36 (Previously Presented): The semiconductor device of claim 35, wherein the plurality of terminals of said CSP type semiconductor device are coupled to the wiring patterns via solder joints.

Claim 37 (Previously Presented): The semiconductor device of claim 34, wherein said CSP type semiconductor device is mounted on said BGA type semiconductor device so that a front surface of said CSP type semiconductor device faces the backside surface of the base plate.

Claims 38-45 (Canceled)

Claim 46 (Previously Presented): The semiconductor device according to claim 34, wherein the main surface of the semiconductor element faces the backside surface of the base plate.

Claims 47-52 (Canceled):

Claim 53 (Previously Presented): A semiconductor device comprising:

a BGA (ball grid array) type semiconductor device including a base plate and a plurality of bumps formed on a backside surface of the base plate; and

a CSP (chip size packaged) type semiconductor device mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have the plurality of bumps formed thereon,

said CSP type semiconductor device having a semiconductor element which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals which are formed on the main surface,

wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed,

wherein the main surface of the semiconductor element is sealed with a resin, and portions of each of the plurality of terminals are exposed from the resin, and

wherein the backside surface of the base plate is mounted to a printed circuit board via the plurality of bumps, and said CSP type semiconductor device as mounted

on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps.

Claim 54 (Previously Presented): The semiconductor device according to claim 53, wherein said BGA type semiconductor device has a plurality of conductive portions on the backside surface of the base plate,

the semiconductor device further comprising a plurality of conductive members, each of which is located between a corresponding one of the plurality of conductive portions and the portion of a corresponding one of the plurality of terminals.

Claim 55 (Previously Presented): The semiconductor device according to claim 54, wherein said conductive members are not sealed with said resin.

Claim 56 (Previously Presented): The semiconductor device according to claim 54, wherein said conductive portions are solder.

Claim 57 (Previously Presented): The semiconductor device according to claim 34, wherein said BGA type semiconductor device has a semiconductor element, a size of the semiconductor element of said BGA type semiconductor device is smaller than a size of the semiconductor element of the said CSP type semiconductor device.

Claim 58 (Previously Presented): The semiconductor device according to claim 34, wherein said BGA type semiconductor device and said CSP type semiconductor device are individually manufactured.

Claim 59 (New): The semiconductor device of claim 34, wherein said BGA type semiconductor device has a semiconductor element which has a thickness greater than a thickness of the semiconductor element of said CSP type semiconductor device.

Claim 60 (New): The semiconductor device according to claim 53, wherein said BGA type semiconductor device has a semiconductor element, a size of the semiconductor element of said BGA type semiconductor device is smaller than a size of the semiconductor element of the said CSP type semiconductor device.

Claim 61 (New): The semiconductor device of claim 53, wherein said BGA type semiconductor device has a semiconductor element which has a thickness greater than a thickness of the semiconductor element of said CSP type semiconductor device.

REMARKS

Claims 34-37, 46 and 53-61 are pending in the present application. Claims 59-61 have been presented herewith.

Information Disclosure Statement

As acknowledged on page 3 of the Advisory Action dated February 11, 2008, the Information Disclosure Statement filed on October 30, 2007, has note been entered because it has been filed after the August 21, 2007 mailing date of the Final Fejection. However, since the Information Disclosure Statement as filed on October 30, 2007, was submitted with a certification and corresponding fee, it is not clear why the Information Disclosure Statement has not been entered and considered.

Regardless, the above noted Information Disclosure Statement has been resubmitted concurrently along with this Request for Continued Examination (RCE). The Bessho reference (U.S. Patent Application Publication No. 2001/0014523) as referred to by the Examiner in the Advisory Action dated February 11, 2008, has also been cited in the Information Disclosure Statement. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm that the documents listed therein have been considered and will be cited of record in the present application.**

Request for Personal Interview

Applicants respectfully request the Examiner to contact the undersigned and to schedule a personal interview, prior to preparation of an Office Action responsive to this Amendment.

Claim Rejections-35 U.S.C. 103

Claims 34-37, 46, 53-56 and 58 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin et al. reference (U.S. Patent No. 5,239,198) in view of the Okuno et al. reference (U.S. Patent No. 6,063,646). Applicants respectfully submit that the arguments previously presented with respect to this rejection are incorporated herein. Applicants will further discuss this rejection during the forthcoming personal interview.

Claims 34, 37, 46, 53, 57 and 58 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Inaba et al. reference (U.S. Patent No. 6,166,1443) in view of the Okuno et al. reference. This rejection is respectfully traversed for the following reasons.

Similarly as noted above, Applicants respectfully submit that the arguments as previously presented with respect to this rejection are incorporated herein. This rejection will also be discussed during the forthcoming personal interview.

With further regard to this rejection, the semiconductor device of claim 34 includes in combination among other features that the back surface and the entirety of

the side surfaces of the semiconductor element of the CSP type semiconductor device are exposed.

However, in Fig. 9 of the primarily relied upon Inaba et al. reference, the entirety of second semiconductor chip 24 as mounted on the rear surface of substrate 22 is encapsulated with encapsulation resin 29 so as to be hermetically sealed. This hinders heat radiation. Even assuming arguendo that motivation existed for modifying the structure in Fig. 9 of the Inaba et al. reference to replace second semiconductor chip 24 with the structure shown in Fig. 8 of the Okuno et al. reference, the entirety of the semiconductor element as mounted on the rear surface of the substrate of the combined prior art would be encapsulated with encapsulating resin 29. That is, the combined teaching would not include a semiconductor element of a CSP type semiconductor device wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed. The combined teaching thus fails to meet the features of claim 34. Applicants therefore respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 34, 37, 46, 57 and 58 is improper for at least these reasons.

The semiconductor device of claim 53 includes in combination among other features a CSP type semiconductor device having a semiconductor element, wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed. As noted above, the structure of the combined device includes encapsulating

resin 29 as shown in Fig. 9 of the primarily relied upon Inaba et al. reference. The combined prior art thus fails to meet the features of claim 53. Accordingly, Applicants respectfully submit that the semiconductor device of claim 53 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 53 is improper for at least these reasons.

Claims 59-61

Claim 59 as dependent upon claim 34, features that the BGA type semiconductor device has a semiconductor element which has a thickness greater than a thickness of the semiconductor element of the CSP type semiconductor device. The prior art as taken together, particularly in view of the Okuno et al. reference, does not specifically disclose these features. Claims 59-61 also will be discussed during the forthcoming personal interview.

Conclusion

Favorable consideration and scheduling of a personal interview are respectfully requested.

As noted above, the Examiner is respectfully requested to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss this application during a personal interview.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of an additional two (2) months to February 21, 2008, for the period in which to file a response to the outstanding Office Action. The required fee of $930.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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